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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/828,556	04/05/2001	Anthony P. Mauro	010034	6493

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EXAMINER	
FIELDS, COURTNEY D	
ART UNIT	**PAPER NUMBER**
2137	

DATE MAILED: 06/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/828,556	MAURO ET AL.	
	Examiner	Art Unit	
	Courtney D. Fields	2137	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 are pending.

Specification

2. The amended disclosure has been accepted by the Examiner.

Response to Arguments

3. Applicant's arguments filed 08 March 2006 have been fully considered but they are not persuasive.

4. Referring to the rejection of claim 1, the Applicant contends that the prior art (Boneh et al. in view of Jones et al.) does not teach nor suggest the following underlined portions: accelerating functions of a software application, a high performance processor configured to operate one layer of the multi-layer protocol according to a command from the first processor and a memory accessible to each of the first processor and the high performance processor for passing commands and data between the first processor and the high performance processor. The Examiner respectfully disagrees and asserts that (Boneh et al. in view of Jones et al.) discloses means for implementing cryptographic acceleration function of a software application utilizing the security protocol IPSec (See Jones et al., Column 5, lines 44-53). Data can be transferred among processors operating one layer of the multi-layer protocol such as IPSec and SSL by utilizing operands of the encryption pipeline processor (See Column 6, lines 18-28). Boneh et al. also discloses a high performance processor, such as a digital signal processor, operating on one layer of an SSL protocol (See page 5, Section 0061)

Furthermore, both Boneh et al. and Jones et al. disclose the means for accessible memory to each of the processors passing operands (See Boneh et al., page 5, Section 0062 and Jones et al., Column 7, lines 15-34)

5. Referring to the rejection of claim 7, the Applicant contends that the prior art (Boneh et al. in view of Jones et al.) does not teach nor suggest the following underlined portions: accelerating security protocols, a shared memory, a processor couple to the memory and operating a first portion of a predetermined one of the security protocols, and a high performance processor coupled to the memory and operating a second portion of the predetermined one of the security protocols. The Examiner respectfully disagrees and asserts that (Boneh et al. in view of Jones et al.) discloses means for implementing cryptographic acceleration function of a software application utilizing the security protocol IPSec (See Jones et al., Column 5, lines 44-53). Boneh et al. discloses means for an authentication algorithm wherein the message authentication code (MAC) protects the user passwords against dictionary attacks within transparent encryption. (See Page 4, Section 0054) Jones et al. discloses means for shared memory wherein each processor has access to the data memory space within a processing element. The shared memory is accessible to all processing elements within an encryption algorithm which allows each processor to have one or more encryption algorithms (See Column 7, lines 25-38) Furthermore, both Boneh et al. and Jones et al. disclose the means for a processor coupled to the memory (See Boneh et al., page 2, Section 0024 and Jones et al., page 4, lines 12-18) and a high performance processor coupled to the memory (See Boneh et al., page 5, Section 0061 and Jones et al., Column 6, lines 3-17)

6. Referring to the rejection of claim 12, the Applicant contends that the prior art (Boneh et al. in view of Jones et al.) does not teach nor suggest the following underlined portions: partitioning a multi-layer security services, a shared memory, first and second processor cores coupled to the shared memory, a multi-layer security services protocol partitioned between each of the first and second processor cores, and one or more application program interfaces operated by the first processor core for interfacing between the security services protocol and the second processor core and a modular math function operating on the second processor core. The Examiner respectfully disagrees and asserts that (Boneh et al. in view of Jones et al.) discloses means for partitioning a multi-layer security services by utilizing the web browser and opening an SSL session as shown in Boneh et al., page 2, Sections 0022, 0057-0058) Jones et al. discloses means for shared memory wherein each processor has access to the data memory space within a processing element. The shared memory is accessible to all processing elements within an encryption algorithm which allows each processor to have one or more encryption algorithms (See Column 7, lines 25-38) Jones et al. discloses the means for a multi-layer security services protocol partitioned between each of the first and second processor cores as shown in Column 7, lines 39-64. Furthermore, Jones et al. discloses the means for one or more application program interfaces operated by the first processor core for interfacing between the security services protocol and the second processor core as shown in Column 17, lines 7-12 and a modular math function operating on the second processor core as shown in Column 8, lines 12-67)

7. Referring to the rejection of claim 15, the Applicant contends that the prior art (Boneh et al. in view of Jones et al.) does not teach nor suggest the following underlined portions: accelerating a multi-layer protocol, partitioning a function of a multi-layer protocol in a first processor, distributing the function to a second high performance processor via a memory shared by both first and second processors, performing the distributing the function in the high performance processor and returning a result of the distributed function from the high performance processor via the shared memory. The Examiner respectfully disagrees and asserts that (Boneh et al. in view of Jones et al.) discloses means for implementing cryptographic acceleration function of a software application utilizing the security protocol IPSec (See Jones et al. Column 5, lines 44-53). Jones et al. discloses the means for a multi-layer security services protocol partitioned between each of the first and second processor cores as shown in Column 7, lines 39-64. Jones et al. discloses the means for distributing the function to a second high performance processor via a memory shared by both first and second processors and performing the distributing the function in the high performance processor as shown in Column 6, lines 44-67 and Column 7, lines 1-14) Furthermore, Jones et al. discloses the means for returning a result of the distributed function from the high performance processor via the shared memory as shown in Column 7, lines 25-38.

8. Therefore, claims 1-20 are maintained in view of the reasons above and in view of the reasons below.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boneh et al. (Pub No. 2002/0112167) in view of Jones et al. (US Patent No. 6,088,800).

As per claim 1, Boneh et al. teaches a device for accelerating functioning of a software application having a high overhead protocol, the device comprising: a first processor operating a software application having a one layer protocol (page 5, section 0061), a high performance processor configured to operate one layer of a protocol according to a command from the first processor (page 5, section 0061), and a memory accessible to each of the first processor and the high performance processor for passing commands and data between the first processor and the high performance processor (page 5, section 0062)

However, Boneh et al. does not teach nor disclose a multi-layer protocol. Jones et al. teaches a multi-layer protocol (See column 5, lines 49-53) Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Boneh et al.'s digital signal processing system with Jones et al. accelerating encryption processing system which will allow a secure software application.

As per claim 2, Boneh et al. (as modified by Jones et al.) teaches the first processor operates a multi-layer security protocol (See column 5, lines 49-53)

As per claim 3, Boneh et al. (as modified by Jones et al.) teaches the high

performance processor is configured to operate a mathematical algorithm layer of the multi-layer protocol (See Jones et al., column 7, lines 65-67, Column 8, lines 1-11).

As per claim 4, Boneh et al. (as modified by Jones et al.) teaches the high performance processor further comprises a digital signal processor (See Boneh et al., page 5, section 0061)

As per claims 5 and 6, Boneh et al. (as modified by Jones et al.) teaches the digital signal processor is further configured to operate a modular math function (See Jones et al., column 8, lines 12-67).

As per claim 7, Boneh et al. (as modified by Jones et al.) teaches a device for accelerating security protocols, the device comprising: a security protocol having one or more of an encryption algorithm and an authentication algorithm (See Boneh et al., page 4, section 0054), a shared memory (See Jones et al., column 7, lines 25-38) a processor coupled to the memory and operating a first portion of a predetermined one of the security protocols (See Boneh et al., page 2, section 0024), and a high performance processor coupled to the memory and operating a second portion of the predetermined one of the security protocols (See Boneh et al., page 5, section 0061).

As per claim 8, Boneh et al. (as modified by Jones et al.) teaches the high performance processor operates the second portion of the security protocol in response to a command from the processor and returns an interrupt signal (See Boneh et al., page 5, section 0060).

As per claim 9, Boneh et al. (as modified by Jones et al.) teaches the high performance processor operates the second portion of the security protocol on data from the processor (See Boneh et al., page 5, section 0061)

As per claim 10, Boneh et al. (as modified by Jones et al.) teaches the high performance processor operates the second portion of the security protocol using a modular math function (see Jones et al., column 8, lines 12-67)

As per claim 11, Boneh et al. (as modified by Jones et al.) teaches the processor passes the data to the high performance processor via the shared memory, and the high performance processor returns a result from operating the second portion of the security protocol to the processor via the shared memory (See Jones et al., column 7, lines 25-38)

As per claim 12, Boneh et al. (as modified by Jones et al.) teaches a circuit for partitioning a multi-layer security services protocol, the circuit comprising: a shared memory (See Jones et al., column 7, lines 25-38), first and second processor cores coupled to the shared memory, a multi-layer security services protocol partitioned between each of the first and second processor cores (See Jones et al., column 5, lines 49-53, column 7, lines 39-64), one or more application program interfaces operated by the first processor core for interfacing between the security services protocol and the second processor core (See Jones et al., column 17, lines 7-12), and a modular math function operating on the second processor core (See Jones et al., column 8, lines 12-67)

As per claim 13, Boneh et al. (as modified by Jones et al.) teaches the first and second processor cores are coupled together through the shared memory (See Jones et al., column 7, lines 25-38)

As per claim 14, Boneh et al. (as modified by Jones et al.) teaches the security services protocol further comprises one of an encryption algorithm and an authentication algorithm (See Boneh et al., page 4, section 0054)

As per claim 15, Boneh et al. (as modified by Jones et al.) teaches a method for accelerating a multi-layer protocol, the method comprising: partitioning a function of a multi-layer protocol in a first processor, distributing the function to a second high performance processor (See Boneh et al., page 5, section 0061) via a memory shared by both the first and second processors, performing the distributed function in the high performance processor (See Jones et al., column 6, lines 44-67, Column 7, lines 1-14), and returning a result of the distributed function from the high performance processor via the shared memory (See Jones et al., column 7, lines 25-38).

As per claim 16, Boneh et al. (as modified by Jones et al.) teaches the distributed function further comprises performing the distributed function in response to a command from a first processor (See Jones et al., column 13, lines 7-32)

As per claim 17, Boneh et al. (as modified by Jones et al.) teaches the first processor performs the partitioning of the function. (See Jones et al., column 9, lines 41-62)

As per claim 18, Boneh et al. (as modified by Jones et al.) teaches performing the distributed function comprises operating an algorithm to perform the function. (See Jones et al., column 15, lines 39-55, column 16, lines 47-51)

As per claim 19, Boneh et al. (as modified by Jones et al.) teaches the algorithm is a modular math function (See Jones et al., column 8, lines 12-67)

As per claim 20, Boneh et al. (as modified by Jones et al.) teaches the multi-layer protocol is a security layer (See Jones et al., Column 5, lines 49-53)

Conclusion

1. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Courtney D. Fields whose telephone number is 571-272-3871. The examiner can normally be reached on Mon - Thurs. 6:00 - 4:00 pm; off every Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Emmanuel Moise can be reached on 571-272-3865. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

cdf
May 26, 2006

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